

Diagram illustrating the structure of a matrix-addressed liquid crystal display (LCD) structure, showing the arrangement of electrodes and the selected pixel.

The structure consists of the following components:

- Address electrodes:** A set of electrodes labeled  $A_1, A_2, A_3, A_4, A_5, \dots, A_{m-1}, A_m$ .
- Scan electrodes:** A set of electrodes labeled  $Y_1, Y_2, Y_3, \dots, Y_{n-1}, Y_n$ .
- Sustain electrodes:** A set of electrodes labeled  $X_1, X_2, X_3, \dots, X_{n-1}, X_n$ .

The diagram shows a grid of electrodes. The intersection of the  $A_2$  address electrode and the  $Y_2$  scan electrode is highlighted with a shaded square, indicating the selected pixel. A label "12" points to the intersection of the  $A_1$  address electrode and the  $Y_2$  scan electrode.

FIG. 3

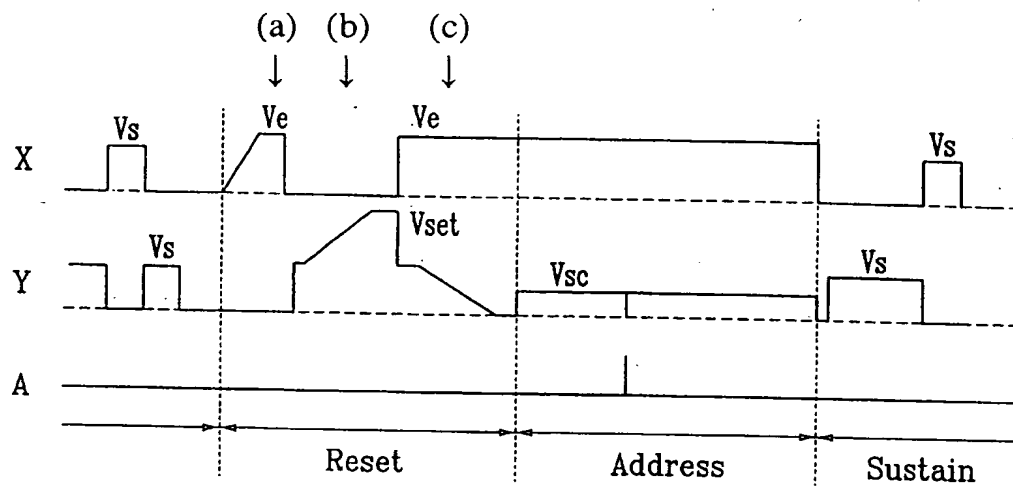


FIG. 4

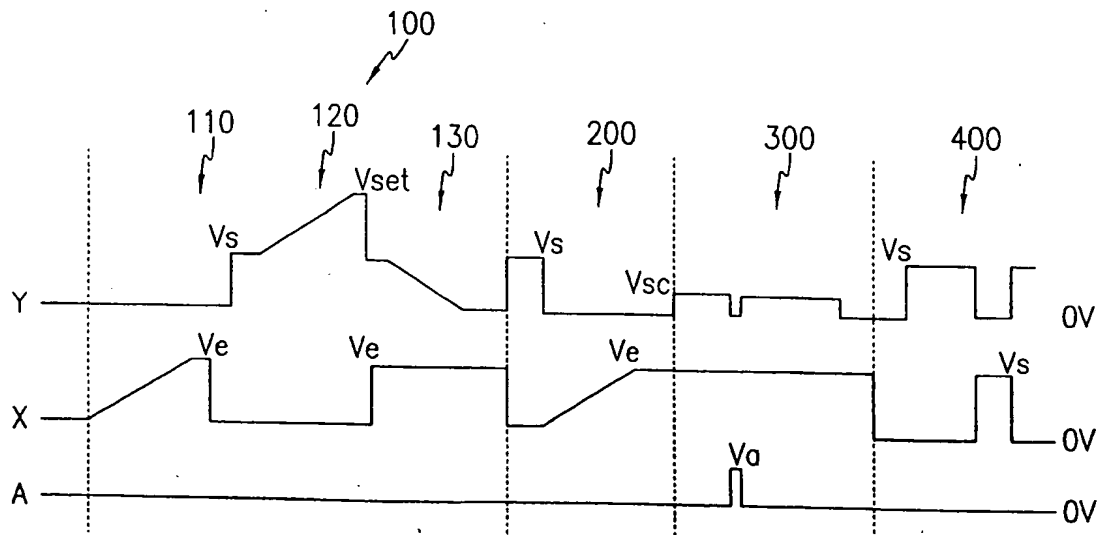


FIG.5A

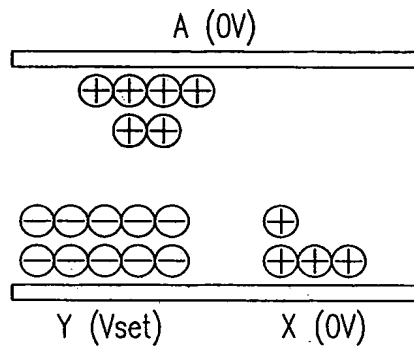


FIG.5B

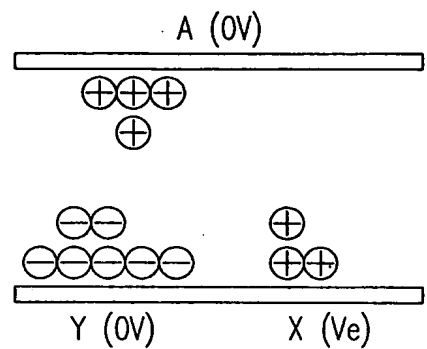


FIG.5C

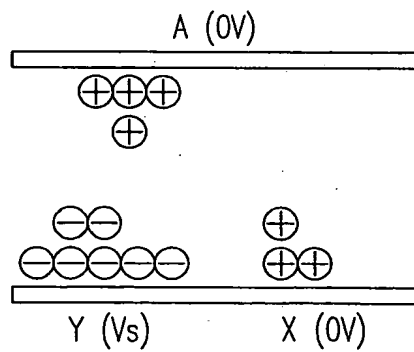


FIG.5D

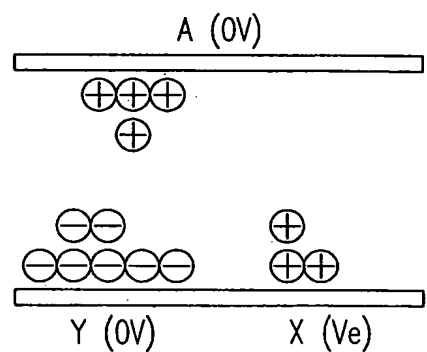


FIG. 6A

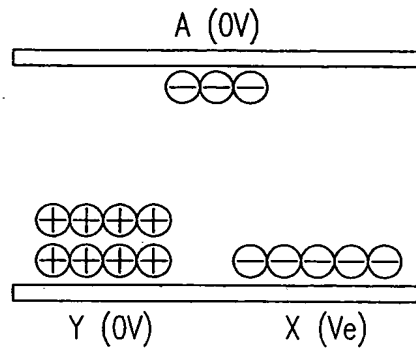


FIG. 6B

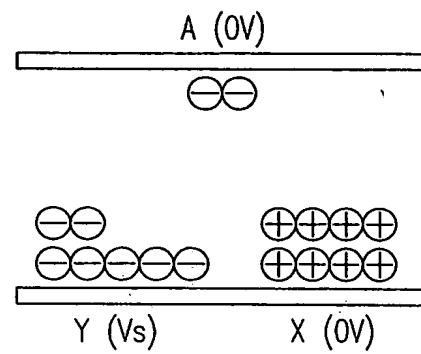


FIG. 6C

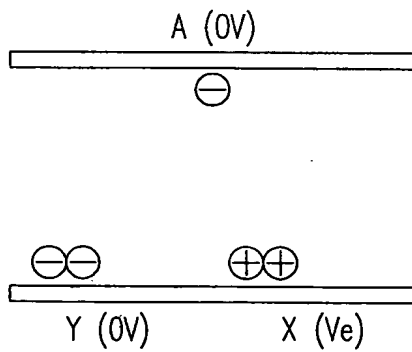


FIG. 7

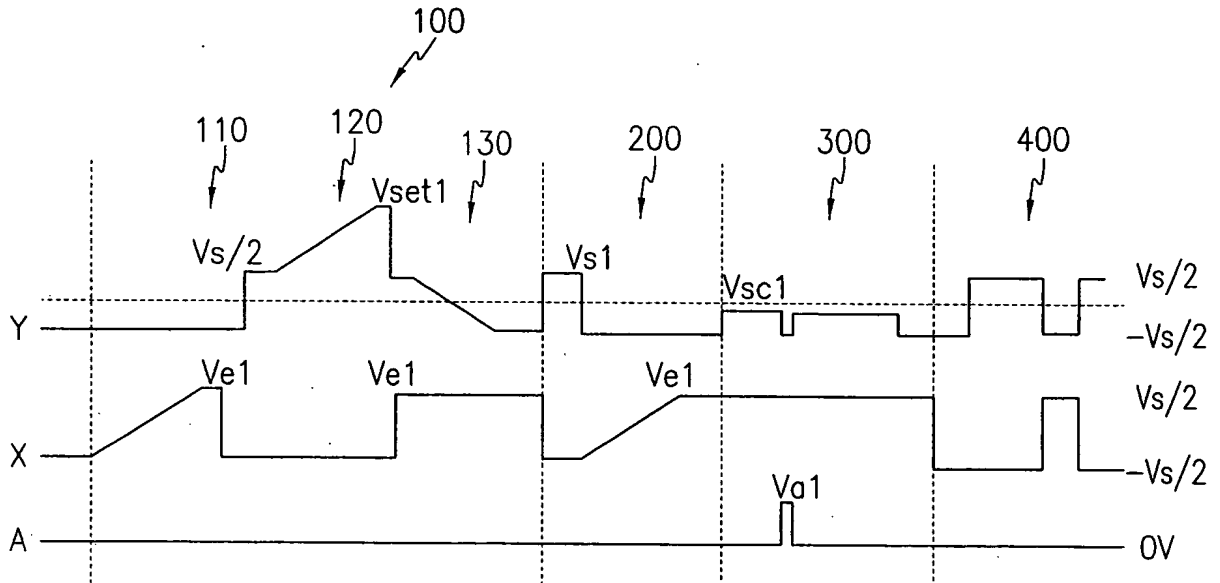


FIG. 8

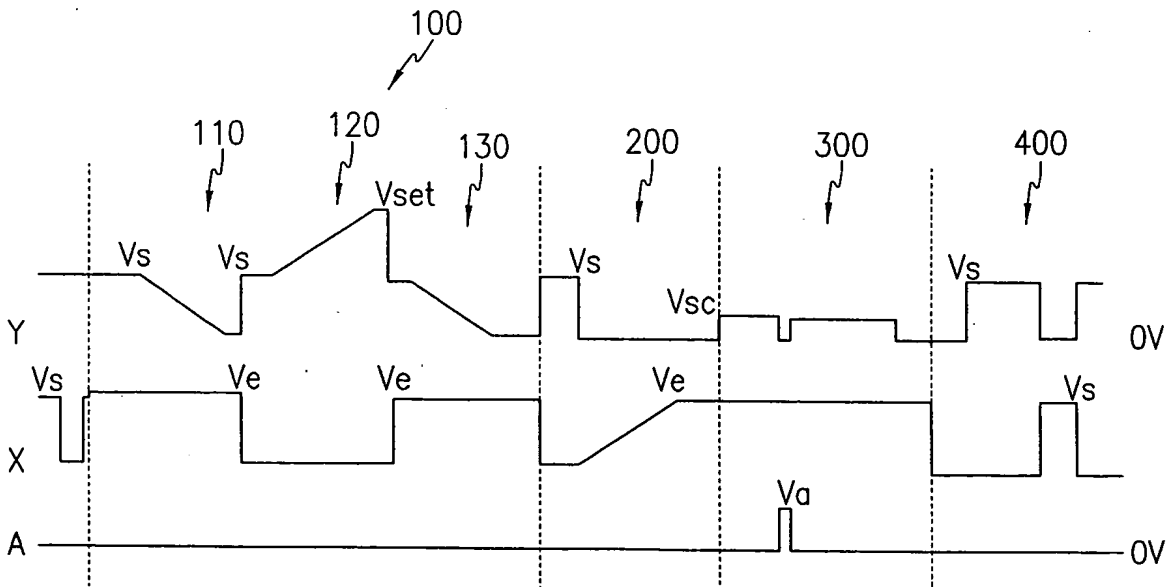


FIG.9

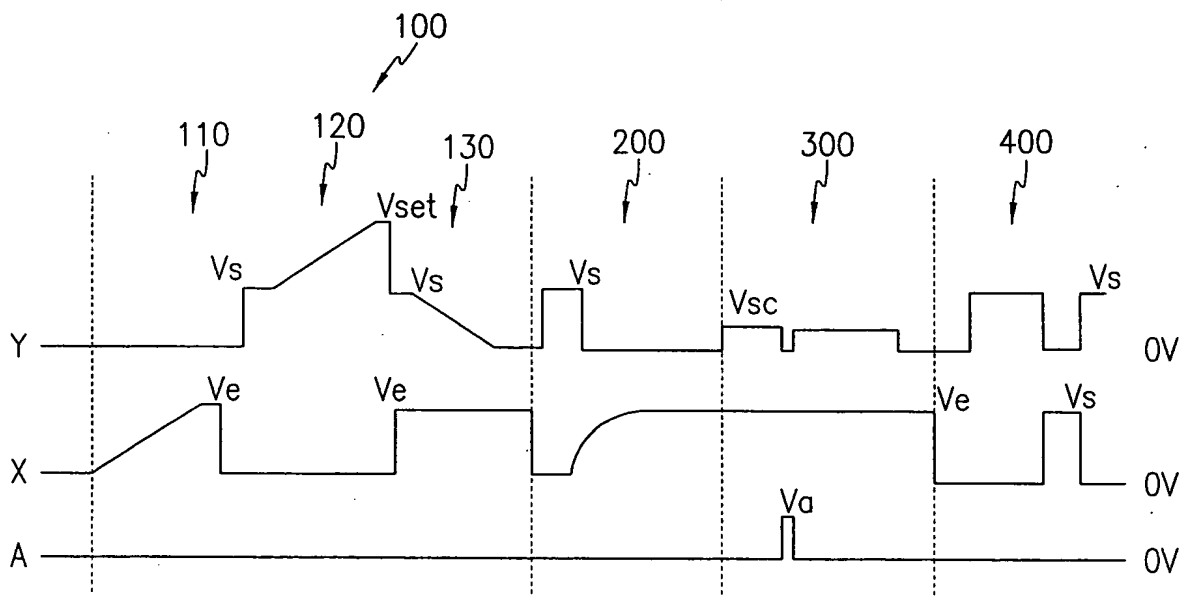
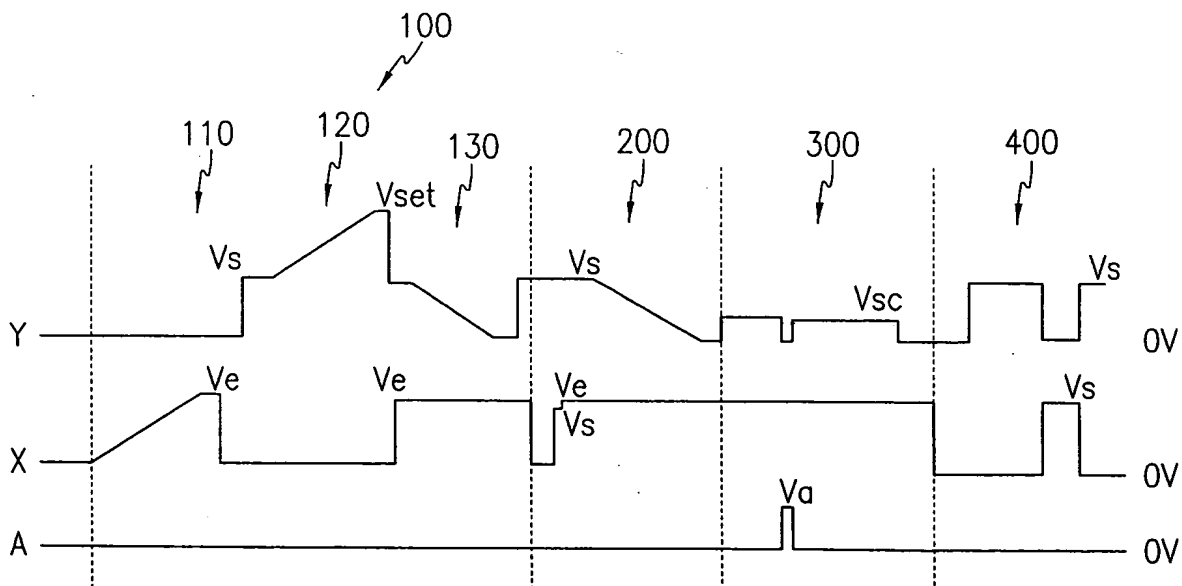


FIG.10



Timing diagram 100 showing signals Y, X, and A over time. The diagram is divided into regions 110, 120, 130, 200, 300, and 400 by vertical dashed lines. Signal Y has levels  $V_s$ ,  $V_{set}$ , and  $V_{sc}$ . Signal X has levels  $V_e$  and  $V_s$ . Signal A has a pulse  $V_a$ . The right side of the diagram is labeled 0V.

FIG.13

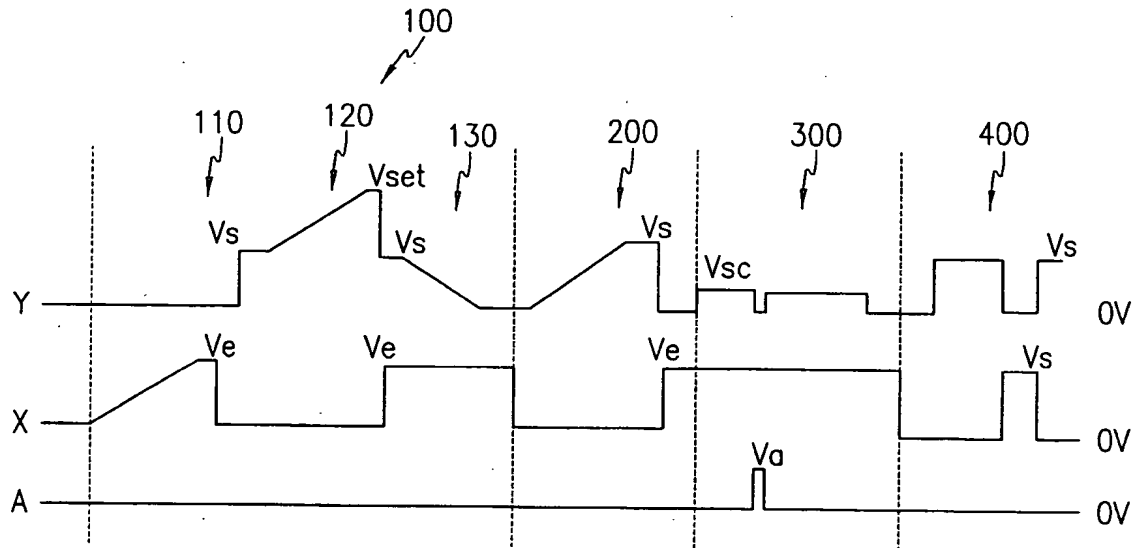


FIG.14

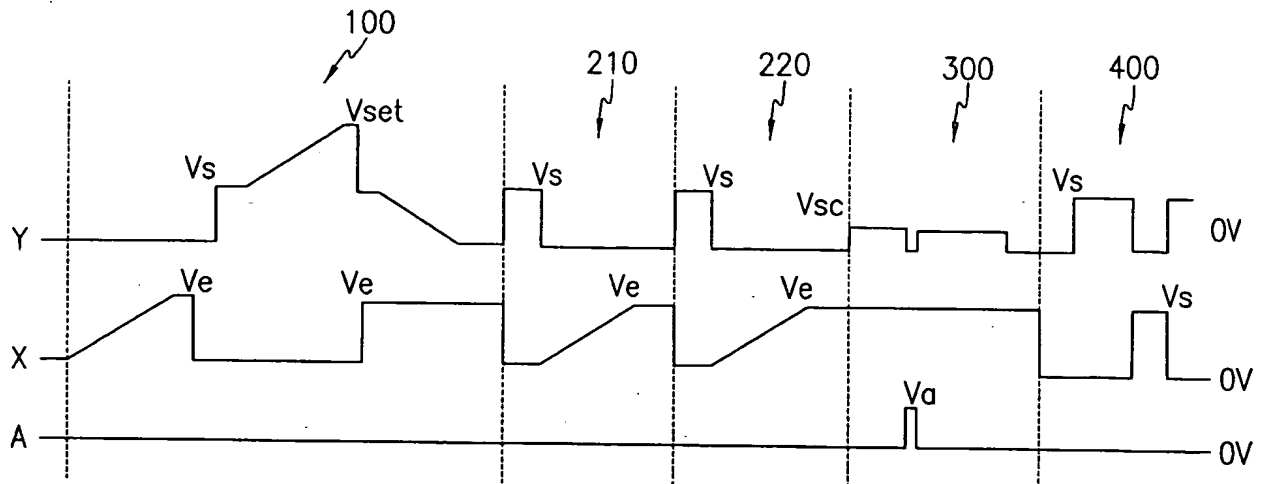




FIG.15

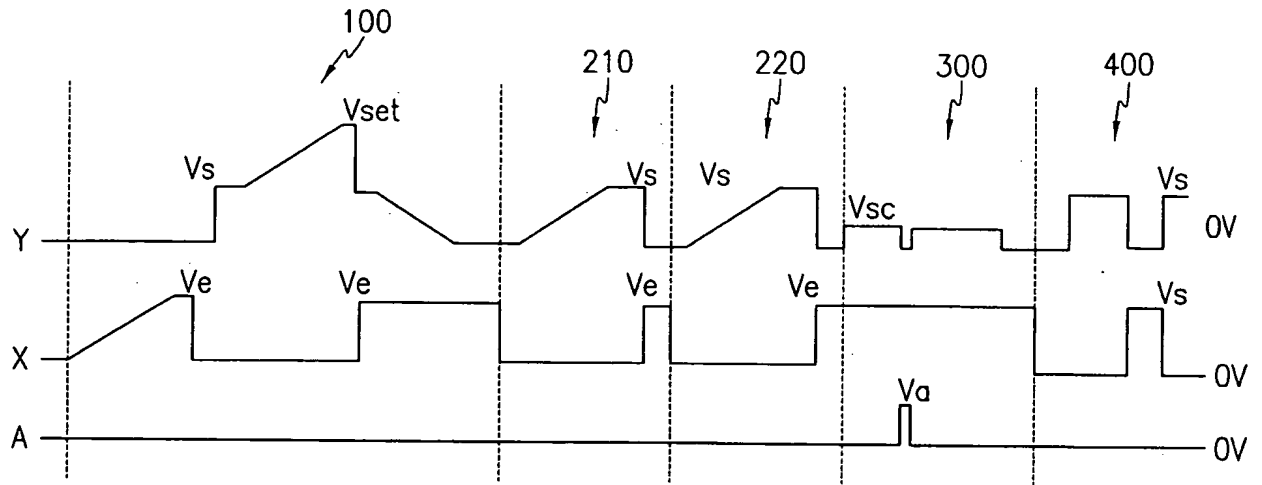


FIG.16

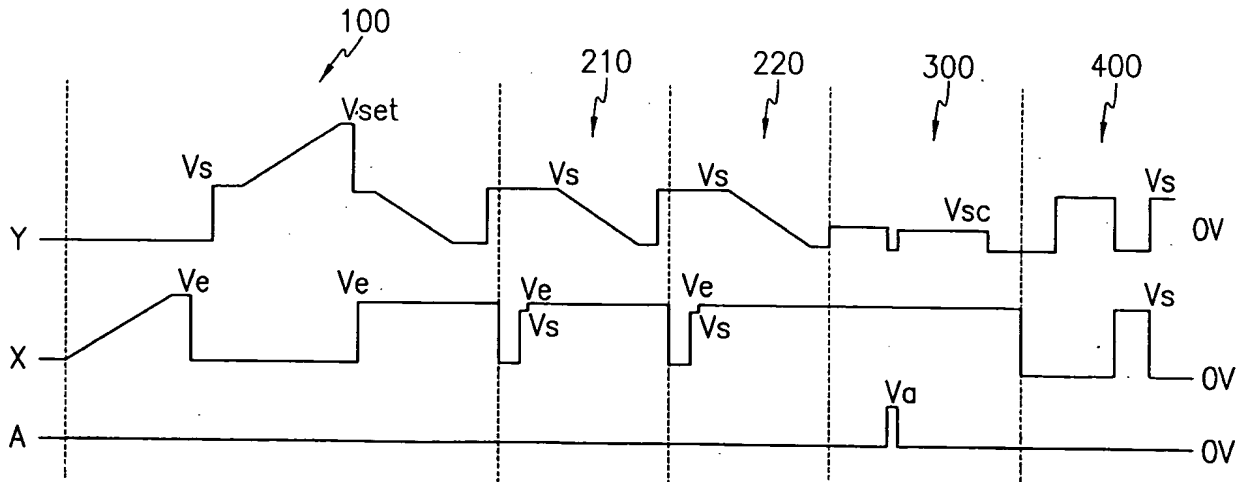


FIG.17

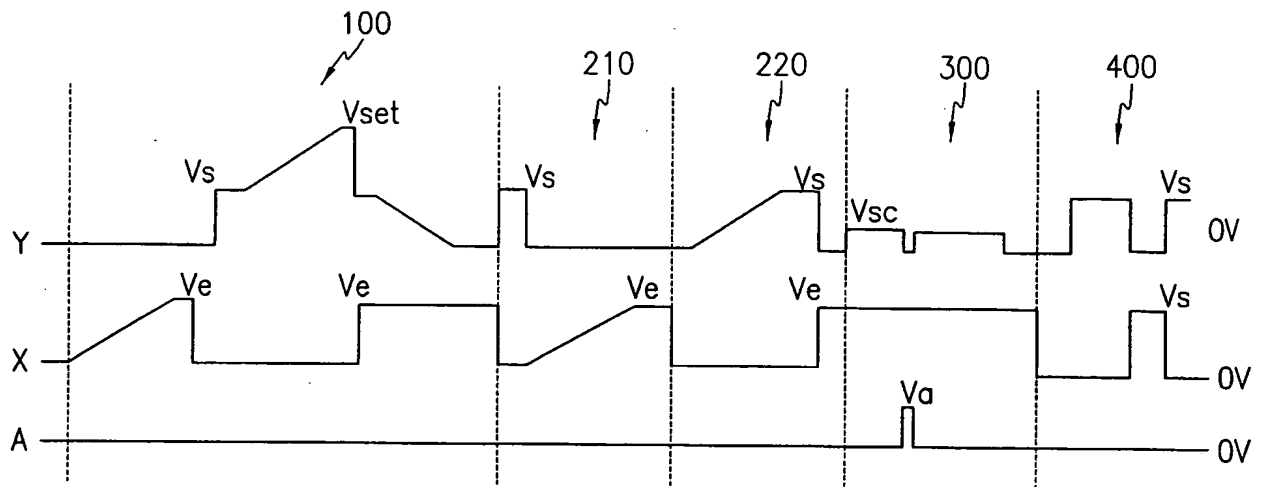


FIG.18

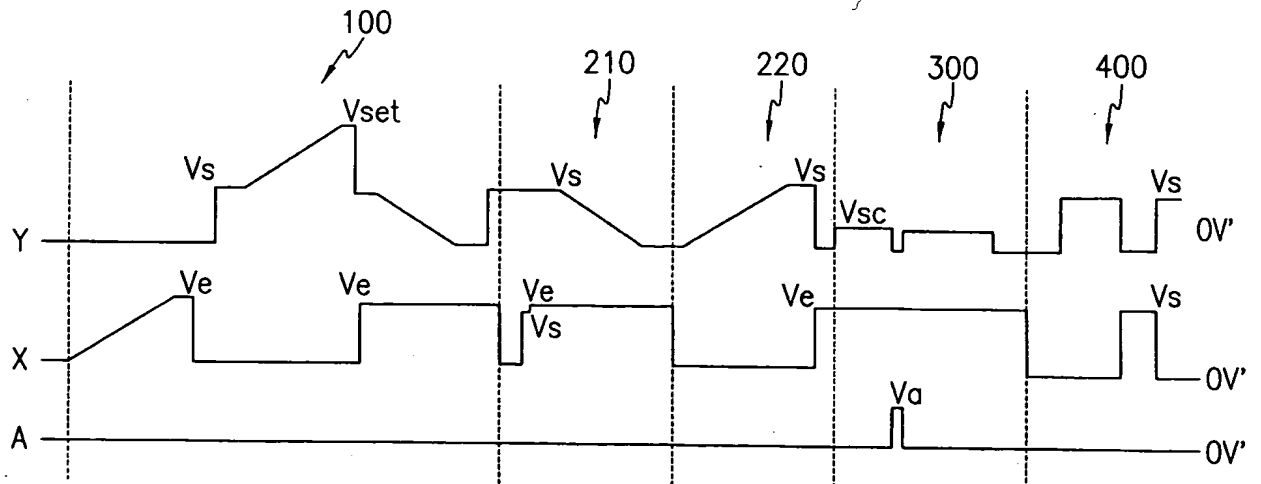


FIG.19

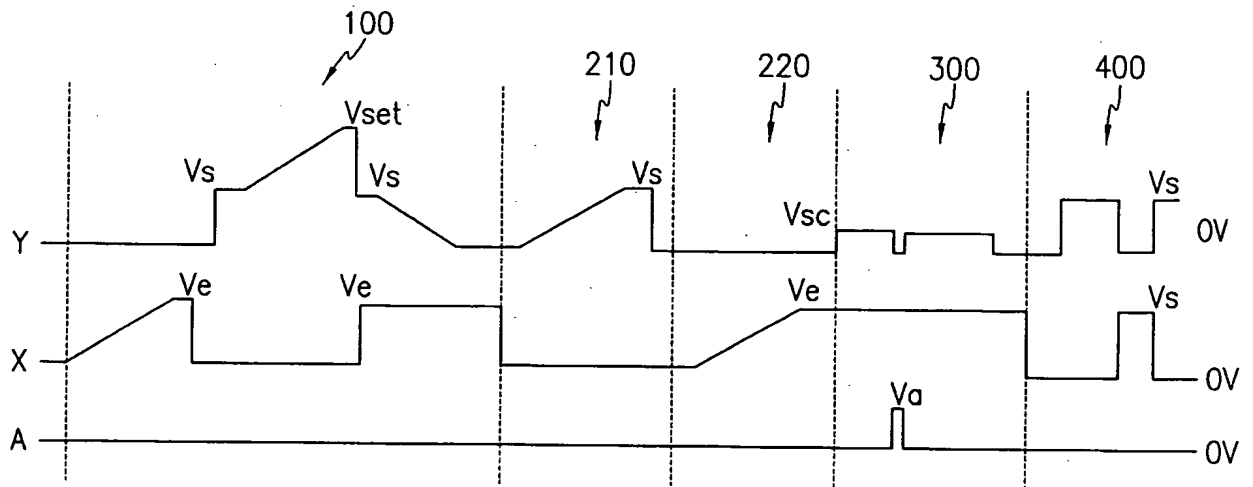


FIG.20

